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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/469,754	12/22/1999	YASUTAKA TSUKAMOTO	2271/53999-A	5345

7590 07/13/2007

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EXAMINER	
CRAIG, DWIN M	
ART UNIT	**PAPER NUMBER**
2123	
MAIL DATE	**DELIVERY MODE**
07/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/469,754	TSUKAMOTO ET AL.	
	Examiner	Art Unit	
	Dwin M. Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-40 have been presented for reconsideration based on Applicants' arguments.

Response to Arguments

2. Applicants' arguments presented in the 4/26/2007 responses have been fully considered; the Examiner's response is as follows:

Regarding the 35 U.S.C. 103(a) rejections of claims 1-40, Applicants' argued on pages 17 and 18 that the cited references fails to teach or suggest that, *"estimation of electrical consumption by integrated circuits which includes among other acts, (i) estimating a current consumed by the mega cells by simulating logic states for each mega cell, (ii) determining an average operation frequency for each logic state, and (iii) estimating a current consumed by the basic cells, as provided by the subject matter of claim 1 of this application."* The Examiner respectfully traverses this argument, Yoichiro clearly teaches *determining an average operation frequency for each logic state, and (iii) estimating a current consumed by the basic cells,* see the machine translation provided with this office action on the forth page is discloses, *"AC power consumption value area which is the 1st storage means which stored AC power consumption value with which 201 is consumed by the element for every state of the element for every element in drawing 2, 202 is the figure having shown AC power consumption value register which is the 2nd storage means which stores the total value of AC consumption value consumed value consumed at the present simulation time. And DC power consumption value area which is the 3rd storage means which stored DC power consumption value with which 203 is consumed by the element for every state of the element for every element, 204 is the figure having shown DC*

power consumption value register which is the 4th storage means which stores the total value of DC consumption value currently consumed at the present time..." see also the figures and text continuing onto the next page. Clearly this teaching of Yoichiro suggests that different circuit elements will have their AC and DC (current) values measured and stored on a computer readable medium, as disclosed by Applicants' expressly argued and claimed limitations. In view of the express teachings and artisan of ordinary skill would apply these methods to mega cells. The Bransen reference was relied upon for a teaching of determining power consumption of mega cells and the Examiner has put forth that in view of the teachings of Yoichiro an artisan of ordinary skill would have been motivated to have taken the new known in the art methods of Yoichiro and modified Bransen to get the claimed methods as disclosed in Applicant's claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1, 9, 17, 25, 29, 33, 37, 38, 39 and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Japanese Laid Open Patent Application Number JP-0105308 to Yoichiro et al. hereafter referred to as Yoichiro in view of U.S. Patent 5,481,469 to Bransen.

3.1 Regarding claims 1, 9, 17, 25, 29, 33, 37, 38, 39 and 40 and using independent claim 1 as an example, Yoichiro substantially teaches, *a computer readable medium including computer executable code stored thereon, the code being executed by a processor to perform a method for estimating power consumption of an integrated circuit comprising: simulating logic of basic* (Figure 3 appears to be a logic NAND gate) *and mega cells of the integrated circuit; estimating a first value of electric power consumed by said mega cells based on said logic simulations* (Abstract [57] "When simulation is started, a DC power consumption value register is initialized on the total value of electric power in a DC power consumption value area 203 to all the elements in a circuit" and Figure 3 shows a logic circuit) *and pre-established power consumption data, including estimating a current consumed by the mega cells by obtaining logic states for each mega cell, determining an average operation frequency for each logic state, and determining an alternating current component* (Abstract[57] "...the power consumption value corresponding to the state of the element is read out of an AC power consumption value...") *and a direct current* (Abstract [57] "A DC power consumption value area to all the elements of the circuit...") *component for each logic state to calculate said current consumed by the mega cells;*

estimating a second value of electric power consumed by said basic cells based on said logic simulations (Abstract [57] "When simulation is started..." and Figure 3 shows a logic circuit) *and pre-established power consumption data, including estimating a current consumed by the basic cells; and combining said first and second value to obtain the power consumption of the integrated circuit* (Patent Abstracts of Japan, Yoichiro, Abstract [57] and Figure(s) 2-6 and the descriptive text).

More specifically the Abstract to Yoichiro teaches, *see the machine translation provided with this office action, "AC power consumption value area which is the 1st storage means which stored AC power consumption value with which 201 is consumed by the element for every state of the element for every element in drawing 2, 202 is the figure having shown AC power consumption value register which is the 2nd storage means which stores the total value of AC consumption value consumed value consumed at the present simulation time. And DC power consumption value area which is the 3rd storage means which stored DC power consumption value with which 203 is consumed by the element for every state of the element for every element, 204 is the figure having shown DC power consumption value register which is the 4th storage means which stores the total value of DC consumption value currently consumed at the present time... "*, see also the remaining text and figures as translated.

However, Yoichiro does not expressly disclose a teaching of simulating and calculating the power consumed by a Mega-cell in an integrated circuit.

Bransen teaches the simulation and calculating of power of a Mega-cell in an integrated circuit (Figures 7 & 8 and Col. 9 lines 38-48).

Yoichiro and Bransen are analogous art because they are from the same problem solving area of calculating power consumption in integrated circuits.

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to have used the power calculation methods of Yoichiro in combination with the Mega-cell power consumption calculation methods of Bransen.

The suggestion for doing so would have been the need to provide accurate calculation of power of logic elements (Bransen Col. 2 lines 1-4) and that in order to accurately account for all power consumed by circuits including mega-cells then the teachings of Bransen are required to predict the power requirements of a Mega-cell circuit.

Therefore, it would have been obvious to combine Bransen with Yoichiro to obtain the invention as specified in claims 1, 9, 17, 25, 29, 33, 37, 38, 39 and 40.

3.2 Regarding claim 40, Yoichiro teaches, *wherein the alternating current component of said current* (Abstract[57] "...the power consumption value corresponding to the state of the element is read out of an AC power consumption value...") *consumed by the mega cells for each logic state is determined by utilizing a predetermined constant value and the average operating frequency for each logic state* (see Figure 6).

However, Yoichiro does not expressly disclose a teaching of simulating and calculating the power consumed by a Mega-cell in an integrated circuit.

Bransen teaches the simulation and calculating of power of a Mega-cell in an integrated circuit (Figures 7 & 8 and Col. 9 lines 38-48).

4. Claims 2-8, 10-16, 18-23, 26-28, 30-32 and 24-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoichiro as modified by Bransen as applied to claims 1, 9, 17, 25, 29, 33, 37, 38, 39 and 40 above and further in view of Microsoft Dictionary Computer Dictionary 1997 edition.

4.1 Yoichiro as modified by Bransen teaches a method of simulating and determining the AC and DC power consumption requirements of integrated circuits as recited in claims 1, 9, 17, 25, 29, 33, 37, 38, 39 and 40 above, differing from the invention as recited in claims 2-8, 10-16, 18-23, 26-28, 30-32 and 24-36 in that their combined teaching lacks,

(claims 2-8, 10-16, 18-23, 26-28, 30-32 and 24-36) storing executable code on a floppy disk, a 3.5 inch floppy disk, a CDROM or Compact Disk a read/write Compact Disk or a DVD disk or where the data therein is compressed.

Microsoft teaches a (3.5 inch floppy disk, page(s) 81 and 201, a CDROM or Compact Disk page 82, a Compact Disk that can read from or written to page 82 and a Digital Video Disk DVD page 145 and compression of data page 107).

Yoichiro as modified by Bransen and Microsoft are analogous art because they are all from the computer technology art.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize 3.5 inch floppy disks, CDROM disks and DVD disks as well as compression because of the these methods of storing executable code were in such wide use that it would be obvious to an artisan of ordinary skill to store and distribute a simulation software program using 3.5 floppy disks, CDROM disks, DVD disks and disks which have compressed data on them.

Conclusion

5. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5.1 A copy of the machine translation of the Yoichiro reference is being provided with this office action.

5.2 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M. Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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